Amendment To The Claims

1. (Previously Presented) A graphics processor, comprising:

a receiving unit for receiving a graphics command from an external unit of the processor;

a transferring unit for performing a data transfer operation to a memory;

a display data generation section including a graphics command storing section for temporarily storing a graphics command which is input through a data bus from the memory, and a decoding section for decoding the graphics command which is output from the graphic command storing section for outputting the generated display data to the memory;

an image display section for receiving the display data from the memory to display an image on a display device;

wherein the graphic command storing section includes at least first data storing means and second data storing means having a check address, reads out graphics commands from selected one of the first and second storing means in a predetermined address order; and when an address of a graphics command is being read out matches a predetermined check address, the graphics processor compares the priority of storing a graphics command to the first data storing means with the priority of the data transfer operation.

2. (Previously Presented) The graphic processor of claim 1, further comprising a bus control section for monitoring a status of use of the data bus and controlling a right to use the data bus,

wherein the bus control section sets a priority for each of at least the following data transfer operations: a data transfer operation of transferring the graphics command to the memory; a data transfer operation of supplying a the graphics command from the memory to the

display data generation section; and a data transfer operation of supplying display data from the memory to the image display section.

3. (Previously Presented) The graphic processor of claim 1, further comprising a bus control section for monitoring a status of use of the data bus and controlling a right to use the data bus,

wherein the bus control section sets a priority for each data transfer operation along the data bus and controls the right to use the data bus according to the set priorities and

wherein the bus control section is configured so that a setting of the priorities of data transfer operations can be changed dynamically.

4. (Previously Presented) The graphic processor of claim 3, further comprising:

a pre-decoding section for pre-decoding a graphics command transferred during a data transfer operation of transferring the graphics command from a CPU to the memory; and

a processing amount estimating section for estimating a data processing amount at the display data generation section based on a result of the pre-decoding by the pre-decoding section,

wherein the bus control section changes the priorities of the data transfer operation according to the data processing amount estimated by the processing amount estimating section.

5. (Previously Presented) The graphic processor of claim 4, wherein when the estimated data processing amount per a predetermined period of time exceeds a predetermined amount, the bus control section sets the priority of a data transfer operation of supplying a

graphics command from the memory to the display data generation section to be higher than the priority of a data transfer operation of transferring the graphics command to the memory.

6. (Previously Presented) The graphic processor of claim 3, further comprising a memory monitor for monitoring an amount of data of graphics commands stored in the memory,

wherein the bus control section changes the priorities of the data transfer operations according to the data amount monitored by the memory monitor.

7. (Previously Presented) The graphic processor of claim 6, wherein when the monitored data amount is smaller than a predetermined amount, the us control section sets the priority of a data transfer operation of transferring an externally-input graphics command to the memory to be higher than the priority of a data transfer operation of supplying a graphics command form the memory to the display data generation section.

8. (Previously Presented) The graphic processor of claim 3, wherein:

the receiving unit is connected to an external bus which is provided external to the graphic processor;

an external bus monitor for monitoring an amount of data being transferred along the external bus is connected to the external bus; and

the bus control section changes the priorities of the data transfer operations along the data bus according to the amount of data being transferred which is monitored by the external bus monitor.

9. Canceled

Claims 10-31 (Cancelled)

32. (Previously Presented) The graphic processor of the claim 1, wherein only when the priority of storing a graphics command to the data storing means is higher, the display data generation section stores a graphics command to the data storing means preferently.

33. (Previously Presented) The graphic processor of the claim 1, wherein the first data storing means and the second data storing means does read out a graphics command simultaneously.

34. (Previously Presented) A graphics processing system of transferring data through a bus comprising:

central processing unit for transferring a graphics command to a memory;

a display data generation section including a graphics command storing section for temporarily storing a graphics command which is input through the data bus from the memory, and a decoding section for decoding the graphics command which is output from the graphic command storing section for outputting the generated display data to the memory;

an image display section for receiving the display data from the memory to display an image on a display device;

wherein the graphics command storing section includes at least first data storing means and second data storing means having a check address, reads out graphics commands from selected one of the first and second storing means in a predetermined address order; and when an

address of a graphics command is being read out matches a predetermined check address, the processor compares the priority of storing a graphics command to the data storing means with the priority of the other data transfer operation.

35. (Previously Presented) The graphic processing system of the claim 34, wherein only when the priority of storing a graphics command to the data storing means is higher, the display data generation section stores a graphics command to the data storing means preferently.

36. (Previously Presented) The graphic processing system of claim 34, wherein the first data storing means and the second data storing means is not able to read out a graphics command simultaneously.

37. (Previously Presented) The graphic processing system of claim 34, wherein the central processing unit, a display data generation section, and a image display section share the bus.

38. (Previously Presented) The graphic processing system of claim 34, wherein a bus control section sets a priority for each of at least the following data transfer operation:

(a) a data transfer operation for transferring the graphics command to the memory through the bus,

(b) a data transfer operation for transferring the graphics command from the memory to the display data generation section through the bus, and

(c) a data transfer operation for transferring the display data from the memory to the image display section through the bus.

39. (Previously Presented) The graphic processing system of claim 38, wherein the data transfer operation for transferring the display data from the memory to the image display section must be given the highest priority at a time interval.

40. (Previously Presented) The graphic processing system of claim 38, wherein the bus control section is configured so that a setting of the priorities of data transfer operations can be changed dynamically.

Claims 41-48 (Canceled).

49. (New) A graphics processor, comprising:

a graphics command storing section for storing a graphics command, including at least first data storage means and second data storing means having a check address; and

a decoding section for decoding the graphics command which is output from the graphic command storing section;

wherein the graphics processor reads out a graphics command from a selected one of the first and second data storing means in a predetermined address order; and when an address of a graphics command being read out matches a predetermined check address, the graphics processor compares the priority of storing a graphics command to the graphics command storing section with the priority of the other data transfer operation.

50. (New) The graphic processor of claim 49, further comprising a bus control section for monitoring a status of use of a data bus and controlling a right to use the data bus,

wherein the bus control section sets a priority for each of at least the following data transfer operations: a data transfer operation of transferring the graphics command to a memory; a data transfer operation of supplying the graphics command from the memory to a display data generation section; and a data transfer operation of supplying display data from the memory to an image display section.

51. (New) The graphic processor of claim 49, further comprising a bus control section for monitoring a status of use of the data bus and controlling a right to use the data bus,

wherein the bus control section sets a priority for each data transfer operation along the data bus and controls the right to use the data bus according to the set priorities and

wherein the bus control section is configured so that a setting of the priorities of data transfer operations can be changed dynamically.

52. (New) The graphic processor of claim 51, further comprising:

a pre-decoding section for pre-decoding a graphics command transferred during a data transfer operation of transferring the graphics command from a CPU to the memory; and

a processing amount estimating section for estimating a data processing amount at the display data generation section based on a result of the pre-decoding by the pre-decoding section,

wherein the bus control section changes the priorities of the data transfer operation according to the data processing amount estimated by the processing amount estimating section.

53. (New) The graphic processor of claim 52, wherein when the estimated data processing amount per a predetermined period of time exceeds a predetermined amount, the bus control section sets the priority of a data transfer operation of supplying a graphics command from the memory to the display data generation section to be higher than the priority of a data transfer operation of transferring the graphics command to the memory.

54. (New) The graphic processor of claim 51, further comprising a memory monitor for monitoring an amount of data of graphics commands stored in the memory,

wherein the bus control section changes the priorities of the data transfer operations according to the data amount monitored by the memory monitor.

55. (New) The graphic processor of claim 54, wherein when the monitored data amount is smaller than a predetermined amount, the bus control section sets the priority of a data transfer operation of transferring an externally-input graphics command to the memory to be higher than the priority of a data transfer operation of supplying a graphics command form the memory to the display data generation section.

56. (New) The graphic processor of claim 51, wherein:

the receiving unit is connected to an external bus which is provided external to the graphic processor;

an external bus monitor for monitoring an amount of data being transferred along the external bus is connected to the external bus; and

the bus control section changes the priorities of the data transfer operations along the data bus according to the amount of data being transferred which is monitored by the external bus monitor.

57. (New) The graphic processor of the claim 49, wherein only when the priority of storing a graphics command to the data storing means is higher, the display data generation section stores a graphics command to the data storing means preferently.

58. (New) The graphic processor of the claim 49, wherein the first data storing means and the second data storing means does read out a graphics command simultaneously.

59. (New) A graphic processor, comprising:

an interface unit for receiving a graphics command from an external unit of the processor and transferring the graphics command to a memory;

a display data generation section for generating a display data from a graphics command in the memory;

a bus control section for controlling a right to use a bus;

a processing amount estimating section for estimating a data processing amount by pre-decoding a data transferring from the interface unit to the memory;

wherein when the estimated data processing amount of the processing amount estimating section exceeds a predetermined amount, the bus control section increases a priority of the graphics command supply operation from the memory to the display data generation section

60. (New) The graphics processor of claim 59, wherein the data processing amount is estimated by obtaining a type of the graphics commands.